Quasi-3D TCAD modeling of STI radiation-induced leakage currents in SOI MOSFET structure

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2D and 3D TCAD modeling is an effective tool for investigating the radiation hardness of various designs and technological solutions of SOI MOSFETs. Radiation degradation assessments of such important MOSFET parameters as threshold voltage (V_{th}), cut-off amplification frequency (f_{max}/f_T), transconductance (S), leakage current (I_{leak}) can be obtained using TCAD modeling.

The traditional 2D MOSFET modeling is sufficient to estimate the radiation dependencies of V_{th}, and f_{max}/f_T. However, the 3D description of the MOSFET structure should be used to determine the leakage current I_{leak}. This is due to the fact that the positive charge Q_{ot} accumulates in a thick SiO_2 layer of shallow trench isolation (STI) and a buried oxide layer (BOX) under the ionizing irradiation. Also, surface states with the N_{it} density at the oxide-silicon interface (SiO_2/Si) are induced. Moreover, the value of Q_{ot} and N_{it} depends on the intensity of irradiation. This leads to inversion of the near-surface layer along STI and BOX, and as the result to the formation of parasitic channels for the leakage current.

Thereby, 3D modeling of the complete MOSFET structure together with STI region (fully 3D) must be carried out. Synopsys Sentaurus TCAD allows carrying out for fully 3D simulation. However, the number of the difference grid elements for calculating the structure is tens of thousands, which, together with the complexity of modeling the charge capture process in the oxide and inversion of the layer in the border region, leads to very large computer time expenditures. For example, the average simulation time of the I-V characteristic for the 3D MOSFET structure with a size W/L=1.5/0.35 μm consisting of 165,000 difference grid elements was 10 hours on a computer with a quad-core Intel i7 (3400 MHz) processor and 16 GB RAM.

As an instrument of a development engineer, fully 3D modeling is unsuitable for the rapid evaluation of the device characteristics in real operating conditions and for calculating a large number of variants, primarily because of the very high expenditure of computer time. Quasi-3D model for calculation of radiation leakage currents in submicron SOI MOSFET structures is proposed. This will make it possible to reduce the computing time by a dozen times and substantially simplify the preprocessor description of the device structure in the TCAD tool.

The traditional 3D modeling of MOSFET structure in the Synopsys TCAD has replaced by the two standard subtasks by modeling the primary MOSFET and parasitic lateral STI structure. Both subtasks are solved independently, the components of the main transistor ($I_{leakMOS}$) and side parasitic transistor ($I_{leakSTI}$) leakage currents are determined, and then these components are summed to determine the total leakage current $I_{leak}=I_{leakMOS}+I_{leakBOX}+I_{leakSTI}$.

0.35 μm SOI MOSFET manufactured using 0.13 μm technology with the following structure parameters L/W=0.35/10 μm, t_{ox}=7 nm, t_{Si}=100 nm, t_{BOX}=145 nm, t_{STI}=130 nm, $N_A=8\cdot10^{17}$ cm^{-3}under the influence of ionizing radiation with a dose of up to 500 krad was simulated. Radiation models based on experimental data obtained for 0.13 μm CMOS technologies were used in modeling to determine the radiation-induced density of N_{ot} defects in SiO_2 oxide layers for BOX and STI regions and on Si/SiO_2 interfaces – N_{it}.

The results of the simulation show that in comparison with the traditional fully 3D modeling, which requires 11 hours of computer time, the computer time for the I_dV_g characteristic was reduced to 71 minutes (i.e. the computer time decreased by 9 times). Simulation for the quasi-3D model are in good agreement with the experimental data, the error in the calculations does not exceed 10%.