Simulation of the super-scalar processor core operation

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Abstract

Modern desktop processors are super-scalar, that is, they are able to perform several operations on several pairs of operands simultaneously. This is achieved by many ways of parallelizing calculations. The main method is the conveyor processing of machine instructions. Each processor contains from one to several cores. Each core contains one to several instruction pipelines. In fact, the pipeline is the heart of the processor. Understanding the mechanism of its work gives an understanding of the principles of computing in modern computers. A huge number of scientific and practical works are devoted to this issue, but a faster and more visual way to study the principle of conveyor processing is the launch and study of the simulation model of the processor core.

In this paper we have built and investigated such a model that allows us to trace the process of executing machine instructions by the processor core pipeline. As a basis for the modeling are taken Intel processor with microarchitecture Nehalem, although the analyzed mechanisms inherent to other modern processors. Modeling system includes the program and methodical recommendations on its use with multiple task options.

The computer model considers as an initial data a fragment of machine code on a simplified Assembler. The fragment consists of twenty instructions. Three main types of machine instructions are considered: data transfer between registers and memory cells (four variations), data processing from registers and memory cells (four variations), conditional jump to the specified address. The simulation program automatically generates a new version of the code fragment at startup or at the user's request. To study the principles of the pipeline, it is additionally proposed to specify the following parameters of the pipeline and the code: the number of store/load devices, the number of ALU (Executive devices), the percentage of memory operations. The modeling kit demonstrates the pipeline architecture consisting of two clusters: front-end and back-end and the principle of translating complex multi-cycle CISC-like instructions into simpler RISC-like micro operations (mops). In addition, it is possible to conduct a more detailed simulation of one of the three mechanisms for calculations accelerating in the processor core: multi-functional processing, out-of-order processing, speculative instructions execution after the branch prediction.

The program includes four Windows of the model, which reflects the input parameters and simulation results. As a result of the simulation program provides the following options:

- to explore the principle of translation of instructions in micro-operation ("MOPs" window),
- to study the employment cycles of the main back-end pipiline cluster when executing the given instructions (the "Pipeline" window»),
- to examine the time diagram of instructions execution from a given code fragment ("Diagram" window).

This modeling kit is useful for studying computer architecture. Understanding the features of the processor is useful for both system developers and programmers. Improving the style of writing programs will speed up their execution by the computer.

References

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