Development of multiprocessor system-on-chip based on soft processor cores schoolMIPS

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At present, there is a trend towards the use of systems-on-chip including a large number of processors, architectural blocks, and peripheral nodes. When designing large-scale multiprocessor systems, a balance should be observed between data transfer rate, amount of resources expended to implement the system, and ability to scale the system without cardinal changes. In such systems, it is extremely inefficient to use a bus topology or a common switch, what made that a new architecture in the form of a network-on-chip (NoC), providing high computational performance and rapid exchange of large data streams, to emerge. In addition, studies of possibilities of using processor cores of MIPS-architecture are becoming more and more urgent, since availability of educational infrastructure of soft processor core MIPSfpga and its simplified version – schoolMIPS – has started to be used in many colleges and universities to teach students computer architecture and hardware-software implementation ofr processor cores using the example of a commercial core.

This work includes a review of MIPS architecture processor cores, as well as comparative analysis of their most famous analogs, such as Nios II, OpenSPARC, RISC-V, openRISC, and MicroBlaze. Also, a comparative analysis of processor interaction subsystems was carried out, which allowed identifying advantages of the network topology consisting of routers over full switch or shared memory topology. A network of routers allows combining heterogeneous cores and blocks on a single chip and also provides simultaneous interaction of multiple blocks which greatly simplifies the topology and removes limitations on its scaling. In addition, the work carried out a review of existing implementations of communication subsystems for NoCs: Xpipes NoC base block library, QNoC with several levels of service quality, MANGO NoC with circuit-level switching for asynchronous data transmission, LRM NoC with multicast data transmission and NoC of 120 simplified microAptiv MIPS processor cores. Most developments support mesh topology and XY routing, and their main difference lies in the architecture of routers.

This work involves realization of 2 multiprocessor systems of 4 and 10 processor cores, developed on NoC topology using schoolMIPS soft-processor cores and routers with XY routing. For networks, mesh topology, providing sufficient network performance, relatively even distribution of load to the nodes, avoiding blockages, and also easy scaling, was chosen. There was implemented partitioning of switching part into input and output blocks connected by the FIFO buffer memory in the router. The arbitrator module controls interaction of the router with the connected processor core and neighboring routers. All messages, arriving at the router, are divided into packets from 1 to 8 flits; each 37 bits in length. Basic processor core schoolMIPS was improved by adding a block of RAM memory, a network interface for interaction of the core with the router, and new instructions and support for external peripherals to its architecture. Network interface is implemented as two separate modules at input and output of the processor core for receiving and transmitting data, respectively.

Maximum operating frequency of the router is 200 MHz, and the throughput reaches 2.13 Gbit / s. Measurement of network performance suggests that a network of 4 processor cores provides a speed of up to 1.87 Gbit / s, and a network of 10 processor cores – up to 1.54 Gbit / s. To implement the router 142 ALMs and 592 bits of memory were consumed; the expanded processor core schoolMIPS consumes 452 ALMs and 1692 bits of memory. The developed NOCs are not too resource-intensive, but they consume enough ALMs: NOC of 4 processor cores takes 2223 ALMs and 9136 bits of memory, and NOC of 10 processor cores – 5696 ALMs and 22840 bits of memory. The obtained results suggest that there is a possibility of NOCs development with the number of nodes up to 50 on Cyclone V SoC 5CSEMA5F31C6 FPGA (Terasic De1-SoC development board) and up to 200 nodes on Stratix IV GX EP4SGX230 (Terasic DE4 development board).