Routing in Networks-on-Chip with Multiplicative Circulant Topology

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Constant increase in complexity of tasks to be solved and in volume of processed information makes it necessary to create complex computing devices consisting of a number of separate processor cores and various peripheral modules; to design such multiprocessor devices, architectural solutions in the field of networks-on-chip (NoCs) are used.

When designing a NOC, it is very important to optimally choose the network topology (a subsystem of processor cores and peripheral devices connection), because it basically determines how effective the NoC is. Usage of suitable topology can significantly increase productivity of the system being developed and reduce its power consumption, as well as chip resources use.

There are lots of topologies for NoC design. Among most effective and promising ones are circulant networks, which belong to regular topologies. In general, the circulant is a graph: $C(N;\ s_1, \dots, s_k)$, where N – number of nodes and s_n – generatrix whose value determines the distance between two nodes. There are lots of different types of circulants, one of which is multiplicative circulant: $C(s^k;\ 1, s, s^2, \dots, s^{k-1}) = MC(s, k)$. It is shown that even with a small network size, circulant topologies have better performance in most important network features compared to widely used mesh topologies. But the topologies, based on multiplicative circulants, have a limited number of variants, because the number of nodes must be strictly a second power of a whole number.

Because multiplicative circulants have a strict, pre-known, geometric form of the network and are characterized by the feature that the lengths of the generatrixes are the powers of one base, a specialized routing algorithm was proposed for such networks that made it possible to simplify the structure of the address part of a packet and to reduce its size. The peculiarity of the proposed algorithm is that when receiving the node number, where the packet is to be delivered, the router of current node does not calculate the whole route, but only the next step. This eliminates the need to store adjacency matrixes which consume significant memory as the number of nodes in the network increases. This is an important advantage of the proposed algorithm in the organization of data transmission in NoC, since memory is an expensive resource in terms of area and power consumption. To calculate the next step, it is enough for the router to store its own number, destination node number, and circulant features – *s* and *k*.

The test performance of the developed algorithm shows that it requires considerably less time for calculations than BFS algorithm does and is easily scalable to large-sized networks. This algorithm calculates steps using mathematical operations and has a linear complexity in contrast to the algorithm of breadth-first search from exponential dependence of the time of path searching on the size of the graph. At the same time, it is simpler than a universal adaptive algorithm for routing in conventional circulants and, accordingly, saves logical resources of the chip.

The above-mentioned algorithm was developed using HDL as part of NoC routers, and its testing in CAD Quartus II, FPGA-based prototyping, and comparison of the obtained results with other routing algorithms for circulant topologies were conducted.